ECE 2049 LECTURE 9

OFFICE HRS

- TONIGHT: 2-6PM
- TUESDAY: 4-6PM

TODAY

- CLOCKS + TIMERS

ADMINISTRIVIA

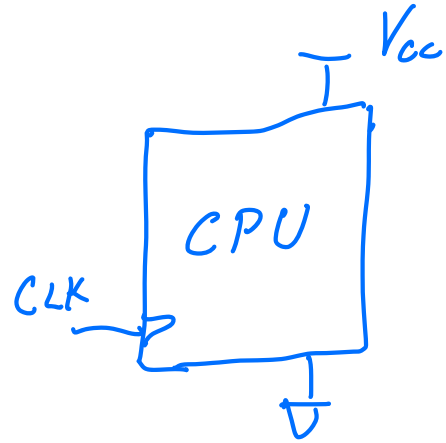
- LAB 2: DUE NEXT WEEK
  - TRY TO GET FIRST STAGES DONE SOON
  -
- HW5: OUT AFTER CLASS

Module 7. Intro to Clocks and Timers

Clocks

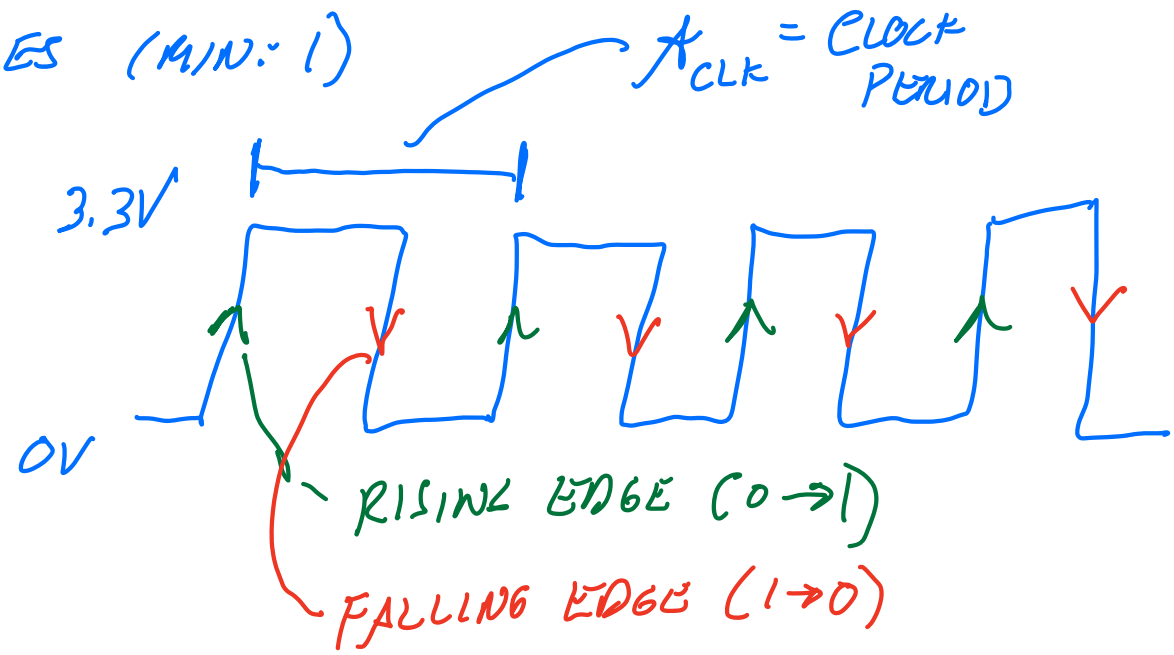
A microcontroller and its peripherals are just sequential logic circuits. Remember that sequential logic circuits need a *clock signal*. Before a CPU can operate, it must have power, a clock signal, and ground.

What does a clock signal look like?



- PROVIDES TIME REFERENCE

- DRIVES EXECUTION OF ALL CPU INSTRUCTIONS
  EVERYTHING EXECUTES IN SOME NUMBER OF CLOCK CYCLES (MIN: 1)



CLOCK FREQUENCY = $1/t_{CLK} = f_{CLK}$

1 CLOCK PERIOD = 1 "TICK"

Clocks on the MSP430: The Unified Clock System (UCS)

Microprocessors usually allow you to configure the clocks used by the system. On the MSP430, this tasks is handled by the **Unified Clock System** (UCS), which is billed as "full featured and capable" (read: complex and confusing)!

Like most microcontrollers, the MSP430 has a variety of configurable *clock sources* and clock *signals*:

SOURCES: CIRCUITS THAT PROVIDE A TIME REF.

⇓

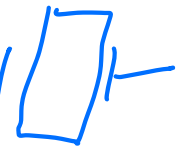
SIGNALS: DRIVE PERIPHERALS + CPU CORE

There are two types of clock sources:

- External sources:

  – OSCILLATOR CRYSTALS (XTAL)

  – CONNECTED TO SPECIAL PINS



- Internal sources:

  – ON-CHIP CIRCUITS THAT MAKE AN OSCILLATOR (NOW? MICRO II)

Why is all of this configurability important?

– PRECISE CONTROL OF CLOCK SPEEDS TO MATCH NEEDS OF APPLICATION

⇒ MAXIMIZE POWER EFFICIENCY!

FASTER IS NOT ALWAYS BETTER IN EMBEDDED SYSTEMS!

The MSP430F5529 has 5 possible clock sources:

XT1CLK LOW-FREQUENCY OSCILLATOR (LFXTAL)
32768 Hz (32.768 kHz)

XT2CLK HIGH-FREQUENCY OSCILLATOR
4 MHz CRYSTAL (HFXTAL)

DCOCLK
→ DIGITALLY CONTROLLED OSCILLATOR

REFOCLK
VLOCLK
→ INTERNAL OSCILLATORS.

These provide 3 clock signals to the CPU and peripherals:

ACLK - Auxiliary Clock:
- USED BY SOME PERIPHERALS
- USUALLY XT1CLK → 32768 Hz

MCLK - Main or Master Clock:
- USED BY CPU (HOW FAST CODE RUNS)
- MSP430: 20 kHz – 20 MHz

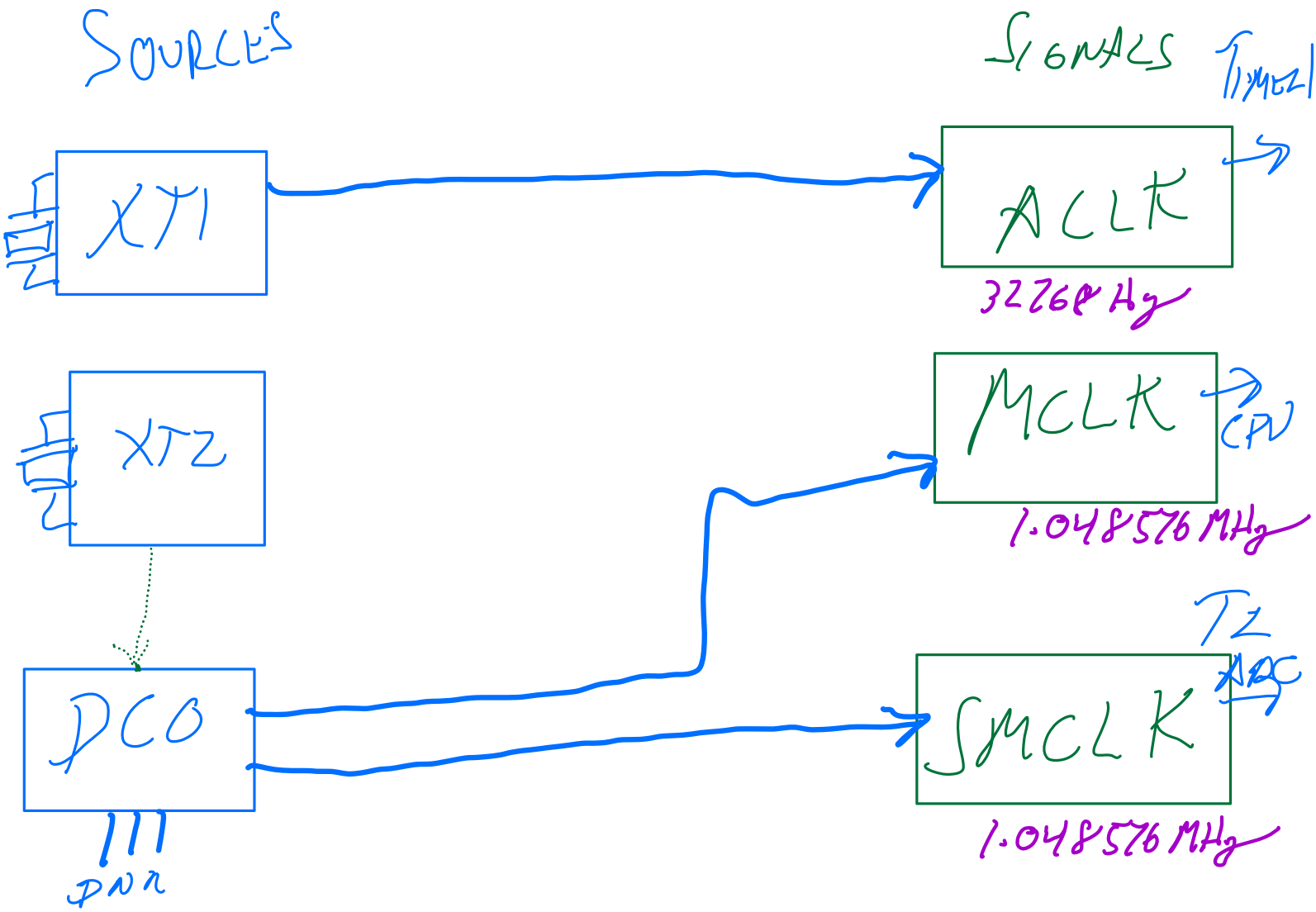
SMCLK - Sub-main Clock:
- USED BY PERIPHERALS
- USUALLY 1.048576 MHz

DEFAULT: 1.048576 MHz

The three clock signals are *software selectable*, meaning that the user can configure the clock sources and speeds for the CPU and peripherals **at runtime**.

Configuring the UCS: The Gist

In general, configuring the UCS boils down to connecting the various clock sources (XT1, XT2, DCO, etc.) to the 3 clock signals (ACLK, MCLK, SMCLK):



In addition, you also need to configure some parameters for the sources (like the DCO), and the signals (like clock dividers).

Configuration notes

Configuring XT1 and XT2

The low frequency and high frequency crystals XT1 and XT2 are connected via pins on the MSP430. On the MSP430F5529, these pins are multiplexed with P5.4-5 (for XT1) and P5.2-3 (for XT2).

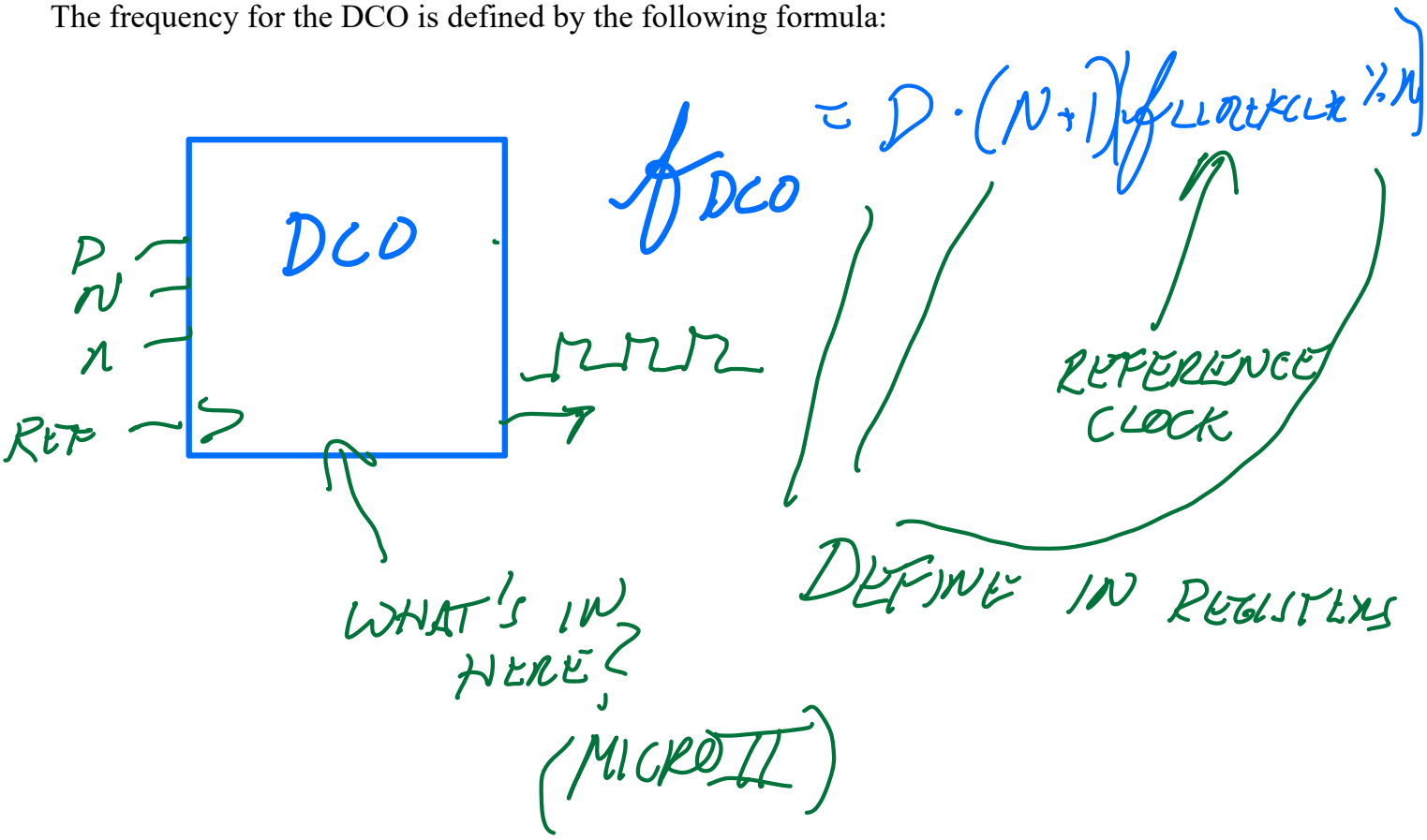
If you want to use XT1 or XT2, you need to configure these pins for **function mode** (as opposed to digital I/O mode) by setting their corresponding bits in P5SEL to 1:

```
P5SEL |= (BIT5|BIT4|BIT3|BIT2);
```

In our lab, this is already done for us in the template in the `configDisplay` function.

The DCO (Digitally-controlled oscillator)

The DCO is a *digitally-controlled oscillator*, which means that you can configure its frequency in software. The UCS module provides a frequency-locked loop (FLL) to stabilize the DCO. The frequency for the DCO is defined by the following formula:



Default clock configuration

After decoding the default register values, we know that **by default**, SMCLK = MCLK, and both use DCOCLK as their source. In addition, ACLK = XT1CLK (if enabled). From this, we can conclude that the default clock settings are as follows:

- ACLK (Auxiliary clock) = 32768 Hz
- MCLK (Master/CPU clock) = 1.048576 MHz
- SMCLK (Sub-main clock) = 1.048576 MHz

In our labs, we will keep it simple and use these default settings! These are important. Remember them!

IN LAB, WE WILL CONFIGURE PERIPHERALS TO USE THESE!