Module 7. Intro to Clocks and Timers

Clocks

A microcontroller and its peripherals are just sequential logic circuits. Remember that sequential logic circuits need a *clock signal*. Before a CPU can operate, it must have power, a clock signal, and ground.

What does a clock signal look like?

Clocks on the MSP430: The Unified Clock System (UCS)

Microprocessors usually allow you to configure the clocks used by the system. On the MSP430, this tasks is handled by the **Unified Clock System** (UCS), which is billed as "full featured and capable" (read: complex and confusing)!

Like most microcontrollers, the MSP430 has a variety of configurable *clock sources* and clock *signals*:

There are two types of clock sources:

- External sources:

- Internal sources:

Why is all of this configurability important?

The MSP430F5529 has 5 possible clock sources:
XT1CLK

XT2CLK

DCOCLK

REFOCLK
VLOCLK

These provide 3 clock signals to the CPU and peripherals:
ACLK - Auxiliary Clock:

MCLK - Main or Master Clock:

SMCLK - Sub-main Clock:

The three clock signals are *software selectable*, meaning that the user can configure the clock sources and speeds for the CPU and peripherals **at runtime**.

Configuring the UCS: The Gist

In general, configuring the UCS boils down to connecting the various clock sources (XT1, XT2, DCO, etc.) to the 3 clock signals (ACLK, MCLK, SMCLK):

In addition, you also need to configure some parameters for the sources (like the DCO), and the signals (like clock dividers).

Configuration notes

Configuring XT1 and XT2

The low frequency and high frequency crystals XT1 and XT2 are connected via pins on the MSP430. On the MSP430F5529, these pins are multiplexed with P5.4-5 (for XT1) and P5.2-3 (for XT2).

If you want to use XT1 or XT2, you need to configure these pins for **function mode** (as opposed to digital I/O mode) by setting their corresponding bits in P5SEL to 1:

```
P5SEL |= (BIT5|BIT4|BIT3|BIT2);
```

In our lab, this is already done for us in the template in the `configDisplay` function.

The DCO (Digitally-controlled oscillator)

The DCO is a *digitally-controlled oscillator*, which means that you can configure its frequency in software. The UCS module provides a frequency-locked loop (FLL) to stabilize the DCO. The frequency for the DCO is defined by the following formula:

Default clock configuration

After decoding the default register values, we know that **by default**, SMCLK = MCLK, and both use DCOCLK as their source. In addition, ACLK = XT1CLK (if enabled). From this, we can conclude that the default clock settings are as follows:

- ACLK (Auxiliary clock) =
- MCLK (Master/CPU clock) =
- SMCLK (Sub-main clock) =

In our labs, we will keep it simple and use these default settings! These are important. Remember them!

Buttons Challenge (from Homework)

What is wrong with this program? What can we do about it?